FIG. 1

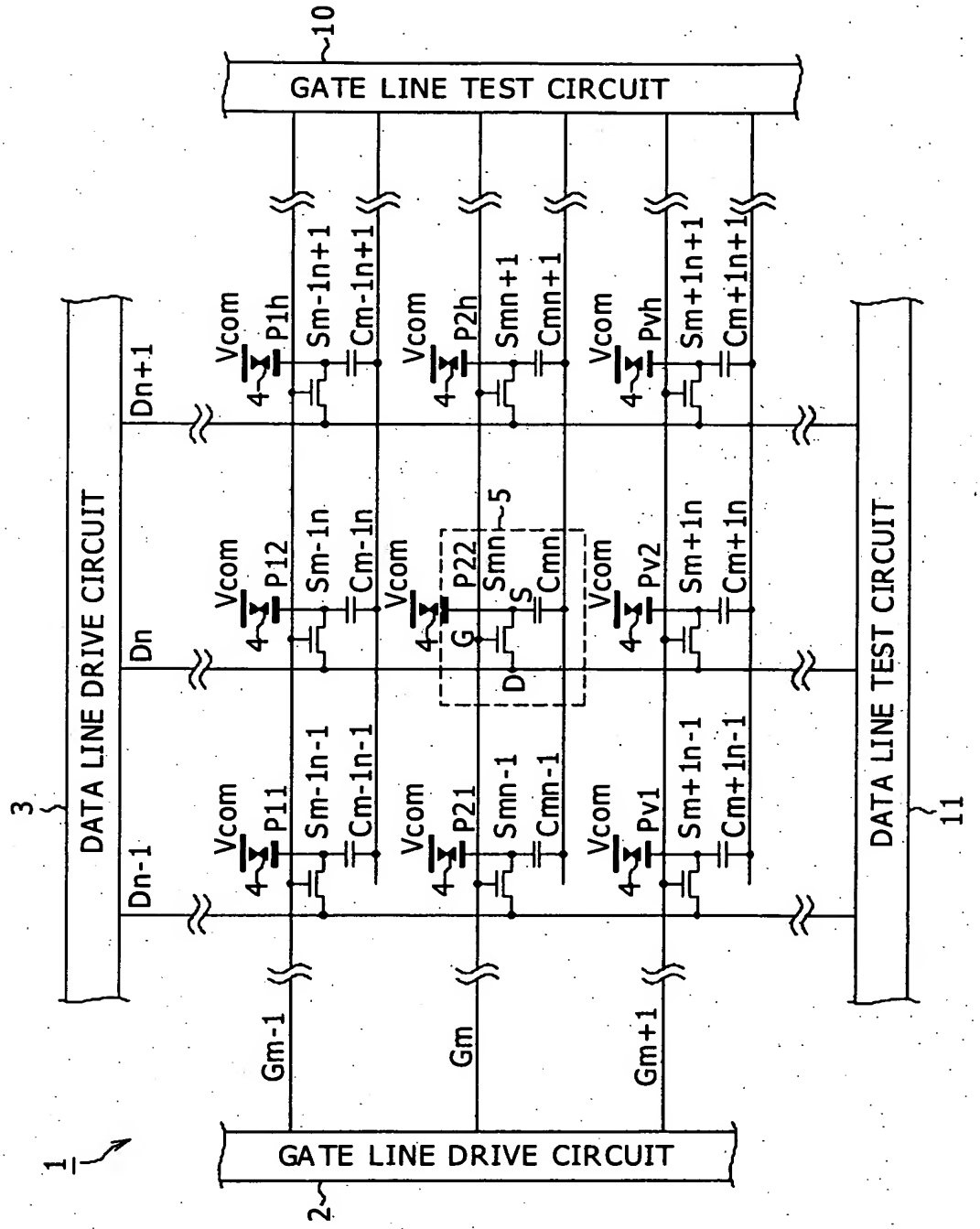

10
GATE LINE TEST CIRCUIT
3
DATA LINE DRIVE CIRCUIT
11
DATA LINE TEST CIRCUIT
2
GATE LINE DRIVE CIRCUIT
1
Dn+1
Dn
Dn-1
Gm-1
Gm
Gm+1
Vcom
4
P1h
P2h
Pvh
P12
P22
Pv2
P11
P21
Pv1
Sm-1n+1
Cm-1n+1
Smn+1
Cmn+1
Sm+1n+1
Cm+1n+1
Sm-1n
Cm-1n
Smn
Cmn
Sm+1n
Cm+1n
Sm-1n-1
Cm-1n-1
Smn-1
Cmn-1
Sm+1n-1
Cm+1n-1
5
G
D
S

FIG. 2

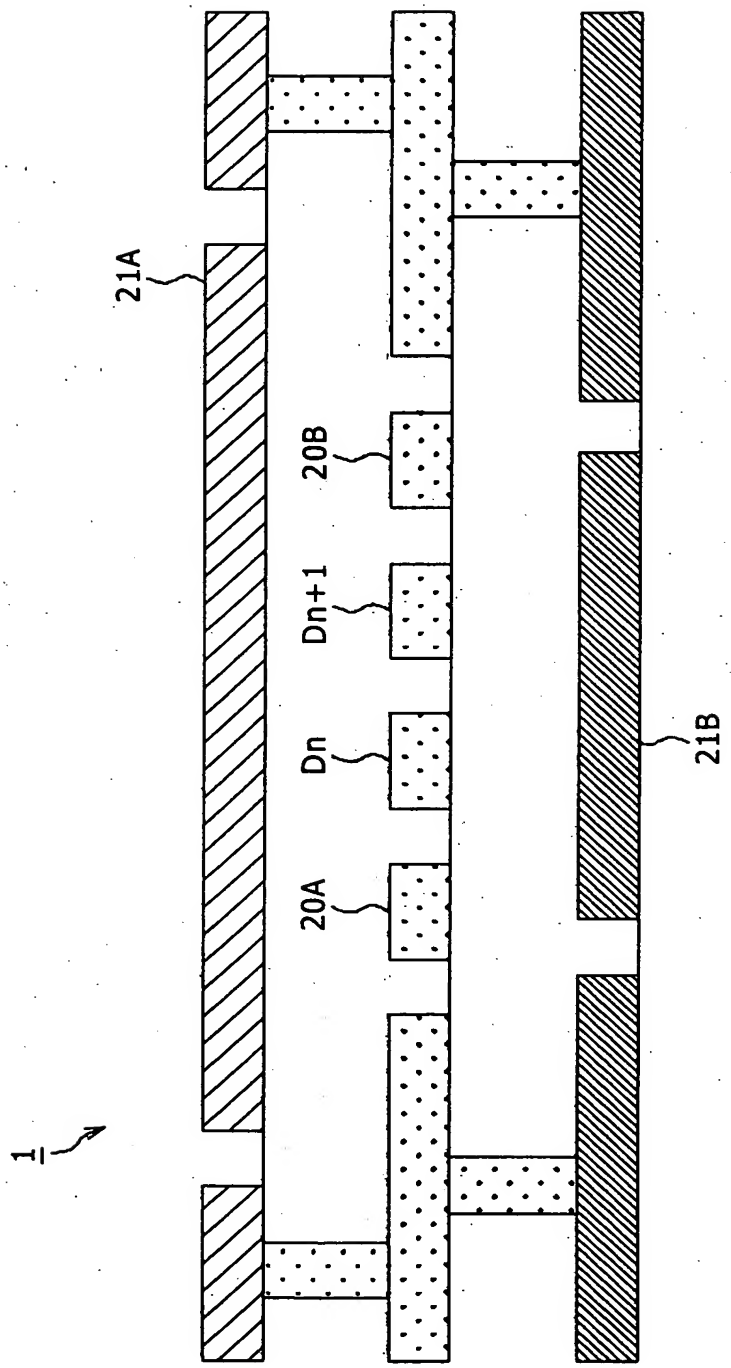


FIG. 3

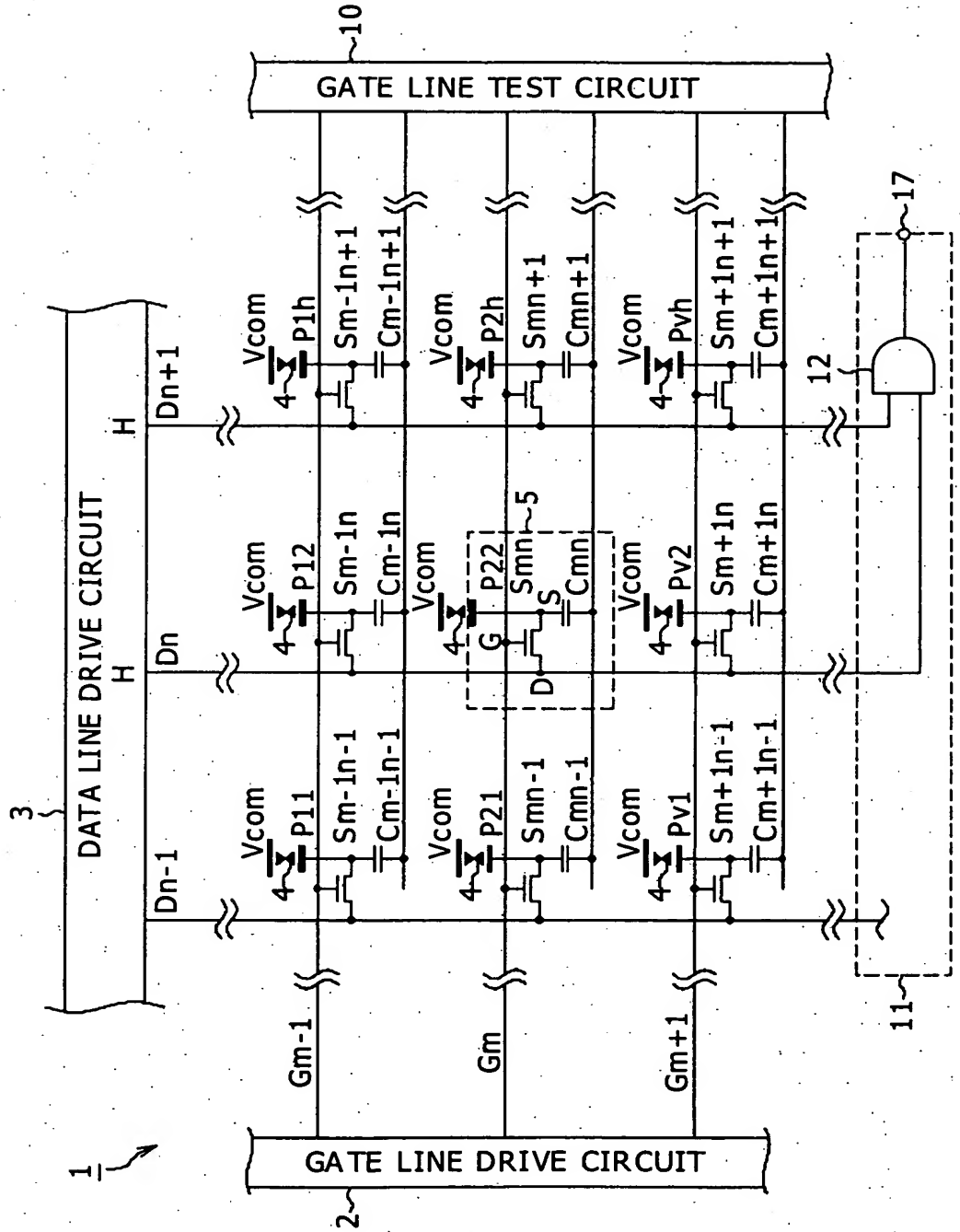

GATE LINE TEST CIRCUIT
10
17
12
11
DATA LINE DRIVE CIRCUIT
3
H
Dn+1
Dn
Dn-1
Vcom
P1h
P2h
Pvh
P12
P22
P11
P21
Pv1
Pv2
Sm-1n+1
Cm-1n+1
Smn+1
Cmn+1
Sm+1n+1
Cm+1n+1
Sm-1n
Cm-1n
Smn
Cmn
Sm+1n
Cm+1n
Sm-1n-1
Cm-1n-1
Smn-1
Cmn-1
Sm+1n-1
Cm+1n-1
5
G
D
S
Gm-1
Gm
Gm+1
GATE LINE DRIVE CIRCUIT
2
1

FIG. 4A

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	OK	H	H
Dn+1	H	OK	H	

FIG. 4B

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	OK	H	L
Dn+1	H	DISCONNECTION	L	

FIG. 4C

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	DISCONNECTION	L	L
Dn+1	H	OK	H	

FIG. 4D

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	DISCONNECTION	L	L
Dn+1	H	DISCONNECTION	L	

FIG. 5

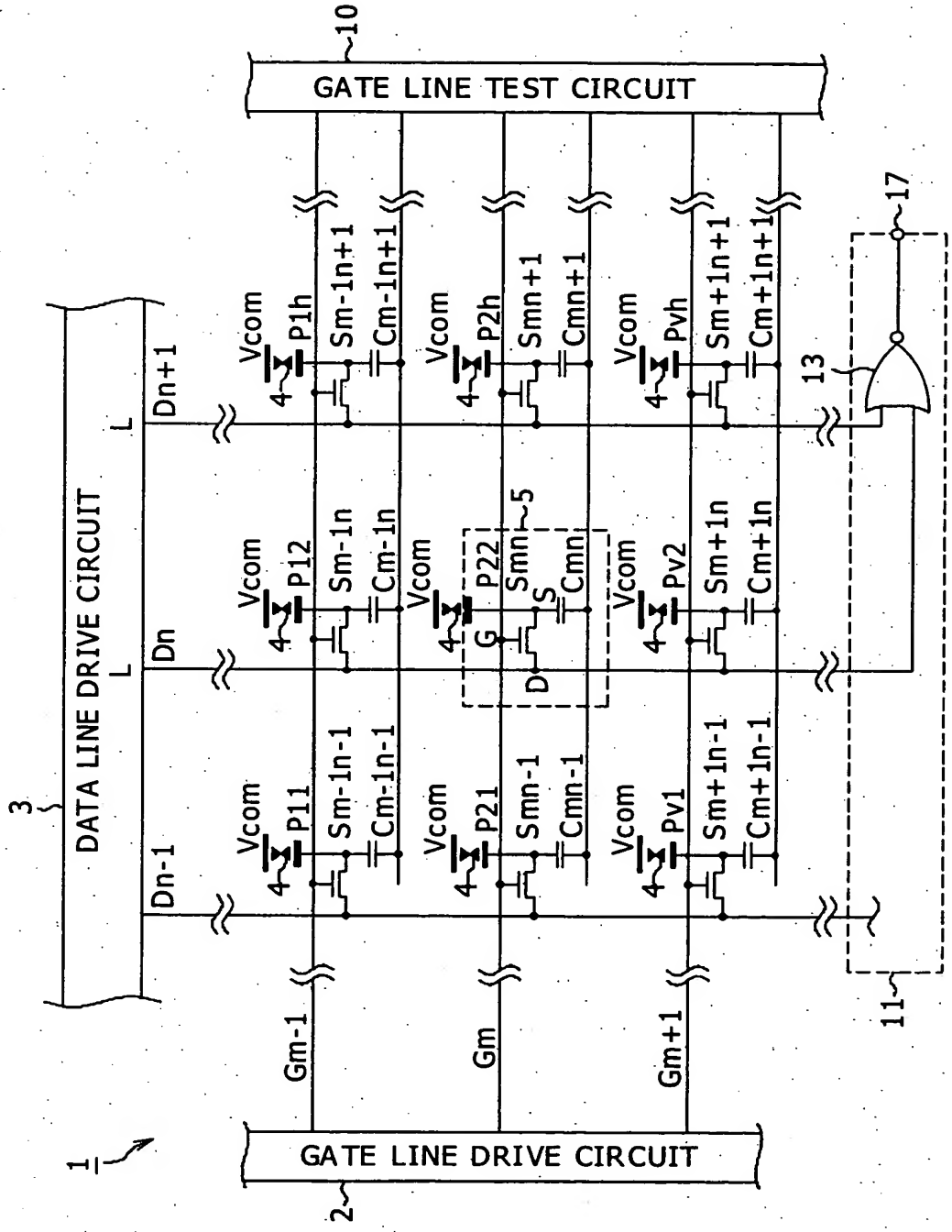

GATE LINE TEST CIRCUIT
10
17
13
DATA LINE DRIVE CIRCUIT
3
Dn+1
Dn
Dn-1
L
Vcom
P1h
P2h
Pvh
P12
P22
Pv2
P11
P21
Pv1
4
Sm-1n+1
Cm-1n+1
Smn+1
Cmn+1
Sm+1n+1
Cm+1n+1
Sm-1n
Cm-1n
Smn
Cmn
Sm+1n
Cm+1n
Sm-1n-1
Cm-1n-1
Smn-1
Cmn-1
Sm+1n-1
Cm+1n-1
5
G
D
S
Gm-1
Gm
Gm+1
GATE LINE DRIVE CIRCUIT
2
1
11

FIG. 6A

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	OK	L	H
Dn+1	L	OK	L	

FIG. 6B

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	OK	L	L
Dn+1	L	DISCONNECTION	H	

FIG. 6C

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	DISCONNECTION	H	L
Dn+1	L	OK	L	

FIG. 6D

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	DISCONNECTION	H	L
Dn+1	L	DISCONNECTION	H	

FIG. 7

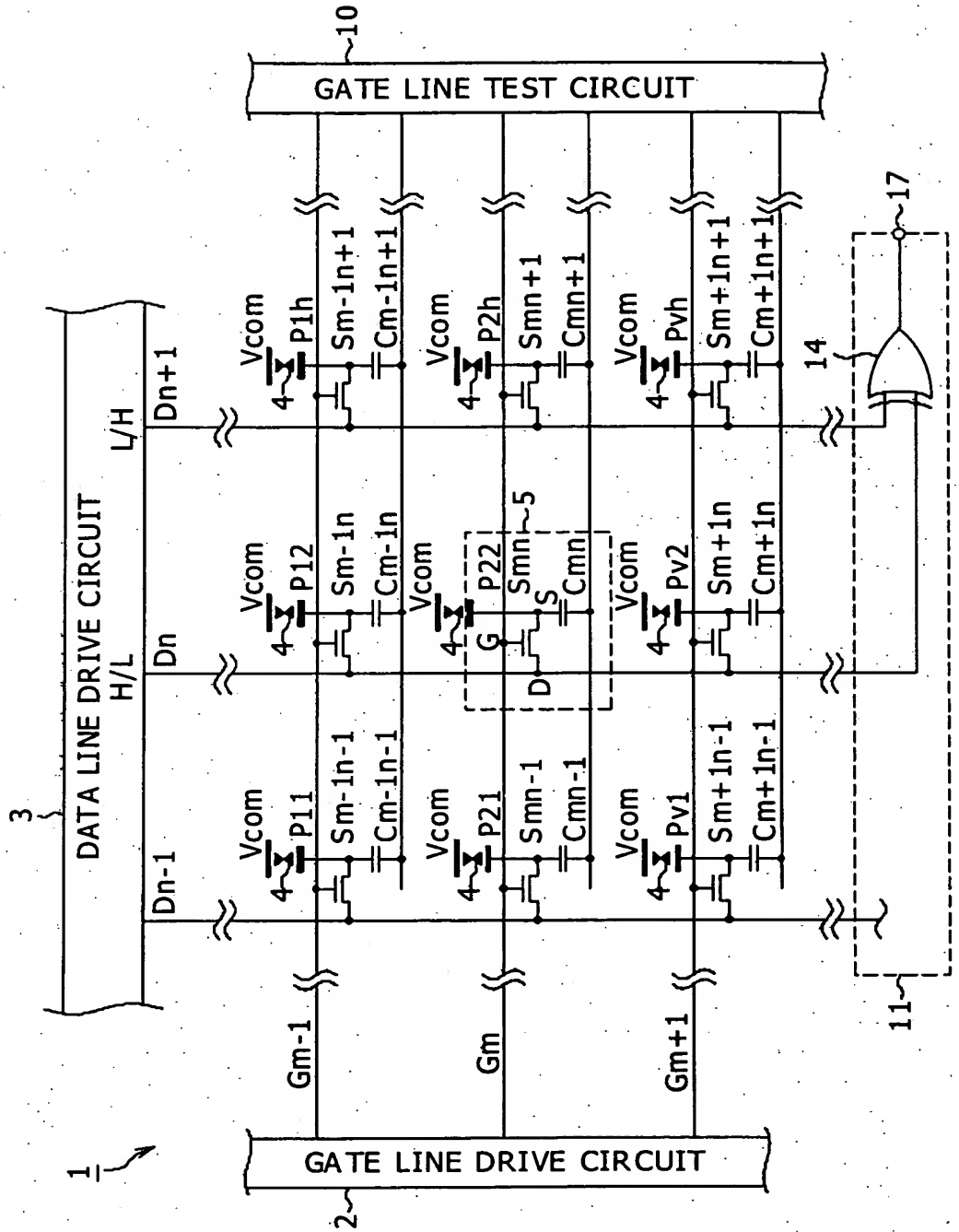

GATE LINE TEST CIRCUIT
10
17
14
DATA LINE DRIVE CIRCUIT
H/L
3
L/H
Dn+1
Dn
Dn-1
Vcom
P1h
P2h
Pvh
P12
P22
Pv2
P11
P21
Pv1
Sm-1n+1
Cm-1n+1
Smn+1
Cmn+1
Sm+1n+1
Cm+1n+1
Sm-1n
Cm-1n
Smn
Cmn
Sm+1n
Cm+1n
Sm-1n-1
Cm-1n-1
Smn-1
Cmn-1
Sm+1n-1
Cm+1n-1
5
G
D
S
4
Gm-1
Gm
Gm+1
11
1
2
GATE LINE DRIVE CIRCUIT

FIG. 8A

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	OK	H	H
Dn+1	L	OK	L	

FIG. 8B

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	SHORT-CIRCUIT (BETWEEN DATA LINES)	L : H	L
Dn+1	L		L : H	

FIG. 8C

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	OK	H	L
Dn+1	L	SHORT-CIRCUIT (H)	H	

FIG. 8D

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	OK	H	H
Dn+1	L	SHORT-CIRCUIT (L)	L	

FIG. 8E

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	SHORT-CIRCUIT (H)	H	H
Dn+1	L	OK	L	

FIG. 8F

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	H	SHORT-CIRCUIT (L)	L	L
Dn+1	L	OK	L	

FIG. 8G

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	OK	L	H
Dn+1	H	OK	H	

FIG. 8H

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	SHORT-CIRCUIT (BETWEEN DATA LINES)	L : H	L
Dn+1	H		L : H	

FIG. 8I

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	OK	L	H
Dn+1	H	SHORT-CIRCUIT (H)	H	

FIG. 8J

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	OK	L	L
Dn+1	H	SHORT-CIRCUIT (L)	L	

FIG. 8K

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	SHORT-CIRCUIT (H)	H	L
Dn+1	H	OK	H	

FIG. 8L

DATA LINE	DRIVE SIGNAL	STATE	GATE INPUT	GATE OUTPUT
Dn	L	SHORT-CIRCUIT (L)	L	H
Dn+1	H	OK	H	

FIG. 9

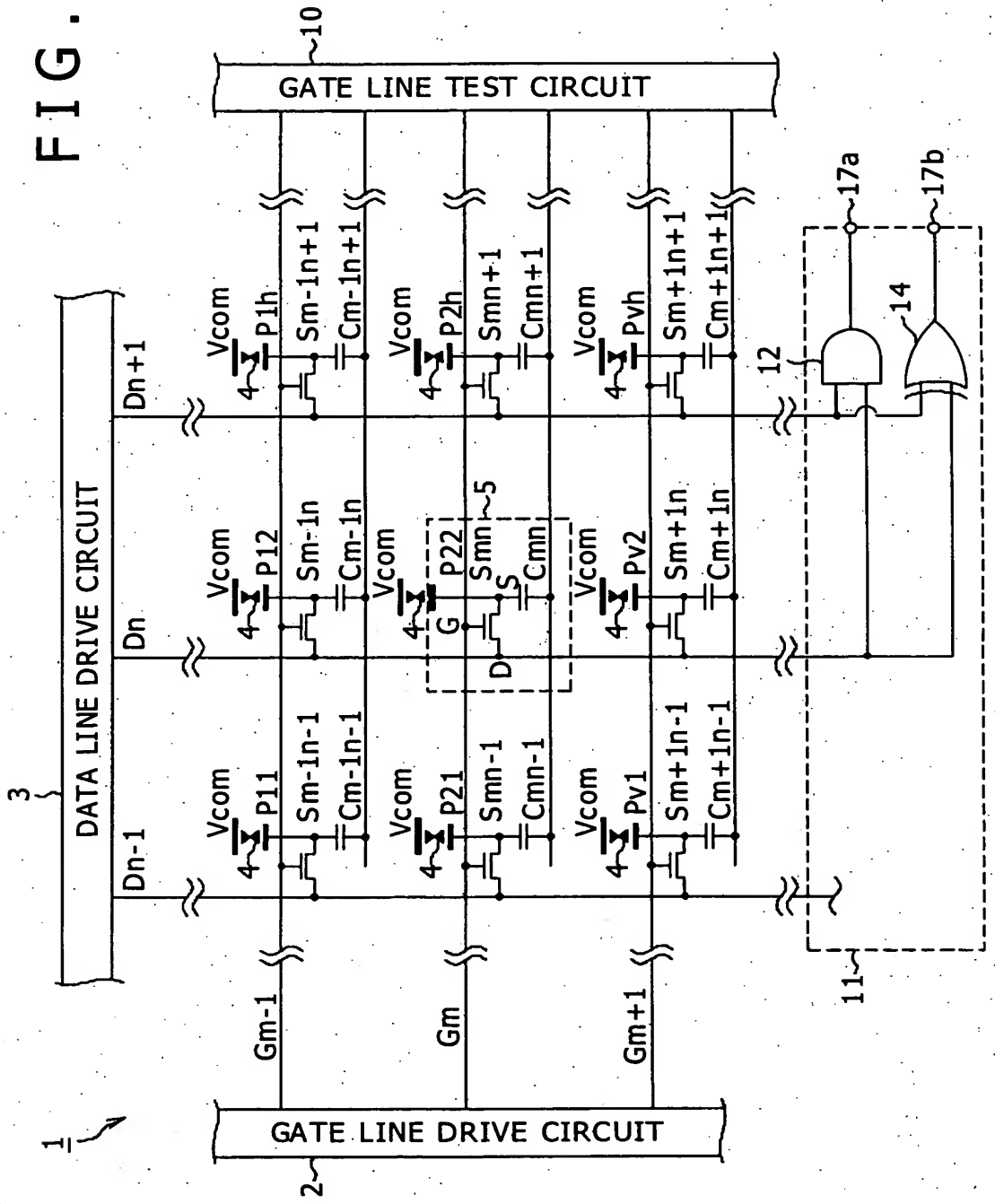

GATE LINE TEST CIRCUIT
10
DATA LINE DRIVE CIRCUIT
3
GATE LINE DRIVE CIRCUIT
2
1
Dn+1
Dn
Dn-1
Gm-1
Gm
Gm+1
Vcom
P1h
P2h
Pvh
P12
P22
Pv2
P11
P21
Pv1
Sm-1n+1
Smn+1
Sm+1n+1
Sm-1n
Smn
Sm+1n
Sm-1n-1
Smn-1
Sm+1n-1
Cm-1n+1
Cmn+1
Cm+1n+1
Cm-1n
Cmn
Cm+1n
Cm-1n-1
Cmn-1
Cm+1n-1
4
5
G
D
S
12
14
17a
17b
11

FIG.10

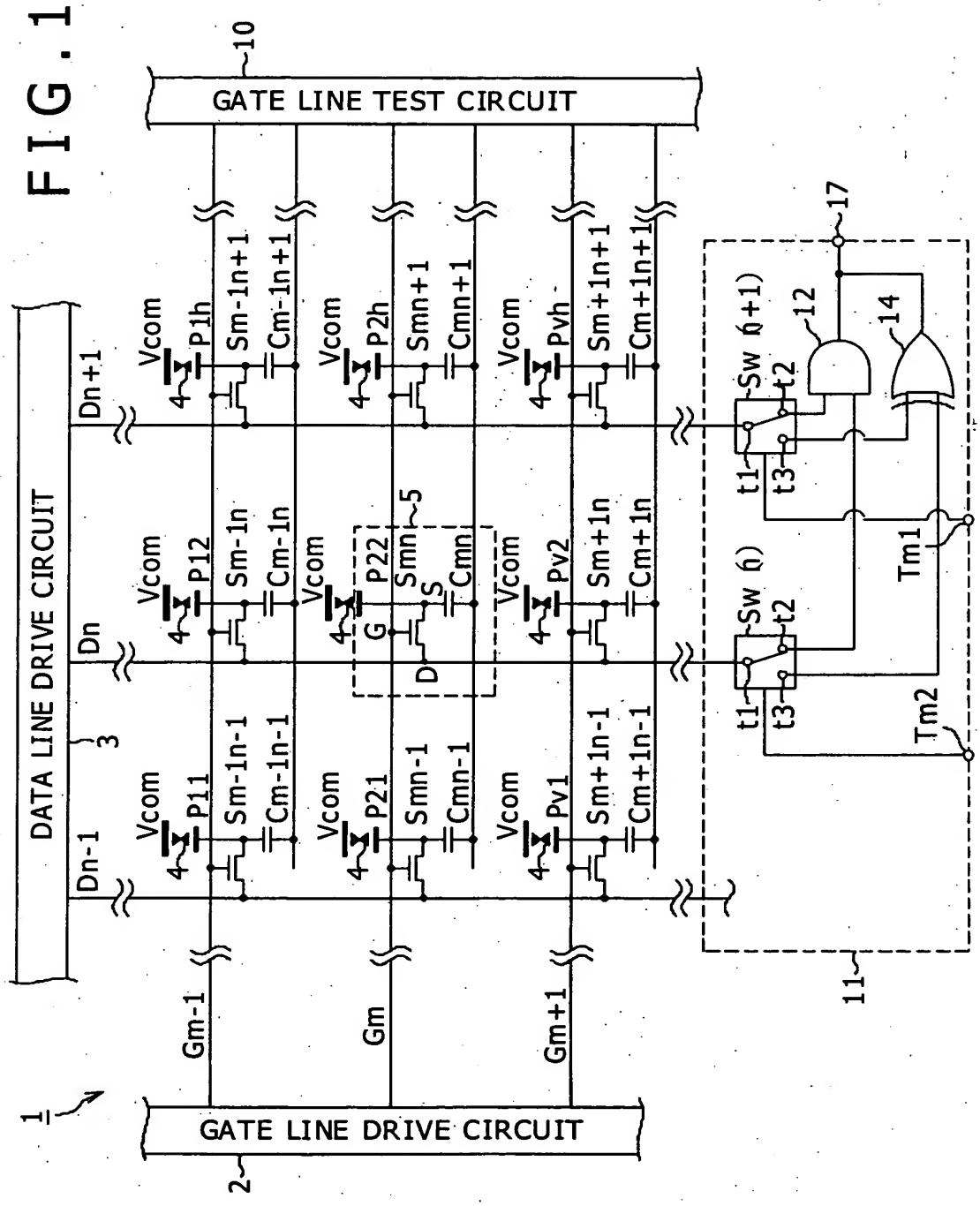

10
GATE LINE TEST CIRCUIT
DATA LINE DRIVE CIRCUIT
3
Dn+1
Dn
Dn-1
Vcom
P1h
P2h
Pvh
P12
P22
Pv2
P11
P21
Pv1
4
5
G
S
D
Sm-1n+1
Cm-1n+1
Smn+1
Cmn+1
Sm+1n+1
Cm+1n+1
Sm-1n
Cm-1n
Smn
Cmn
Sm+1n
Cm+1n
Sm-1n-1
Cm-1n-1
Smn-1
Cmn-1
Sm+1n-1
Cm+1n-1
17
Sw (n+1)
Sw (n)
t1
t2
t3
12
14
Tm1
Tm2
11
Gm-1
Gm
Gm+1
1
2
GATE LINE DRIVE CIRCUIT

FIG. 11

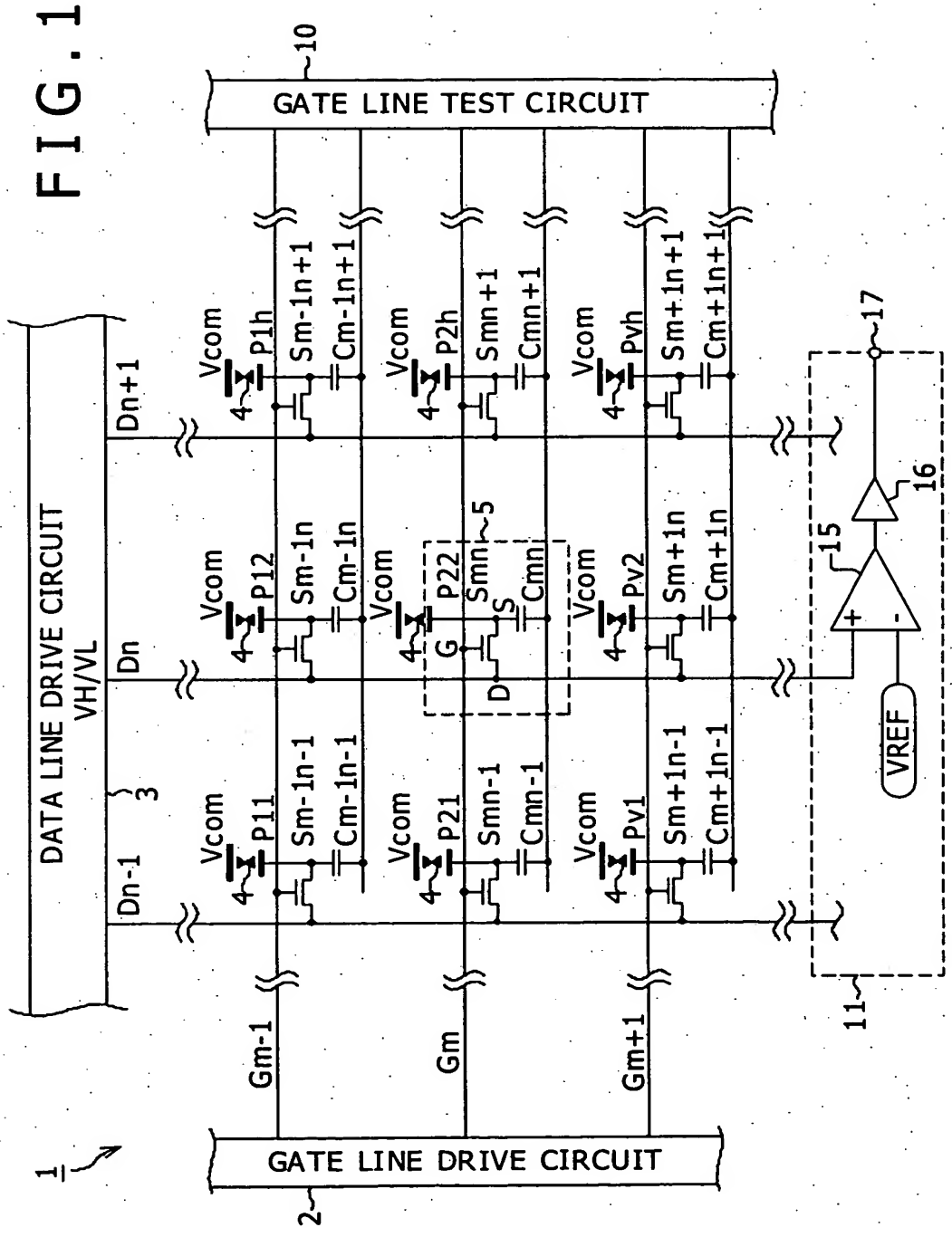
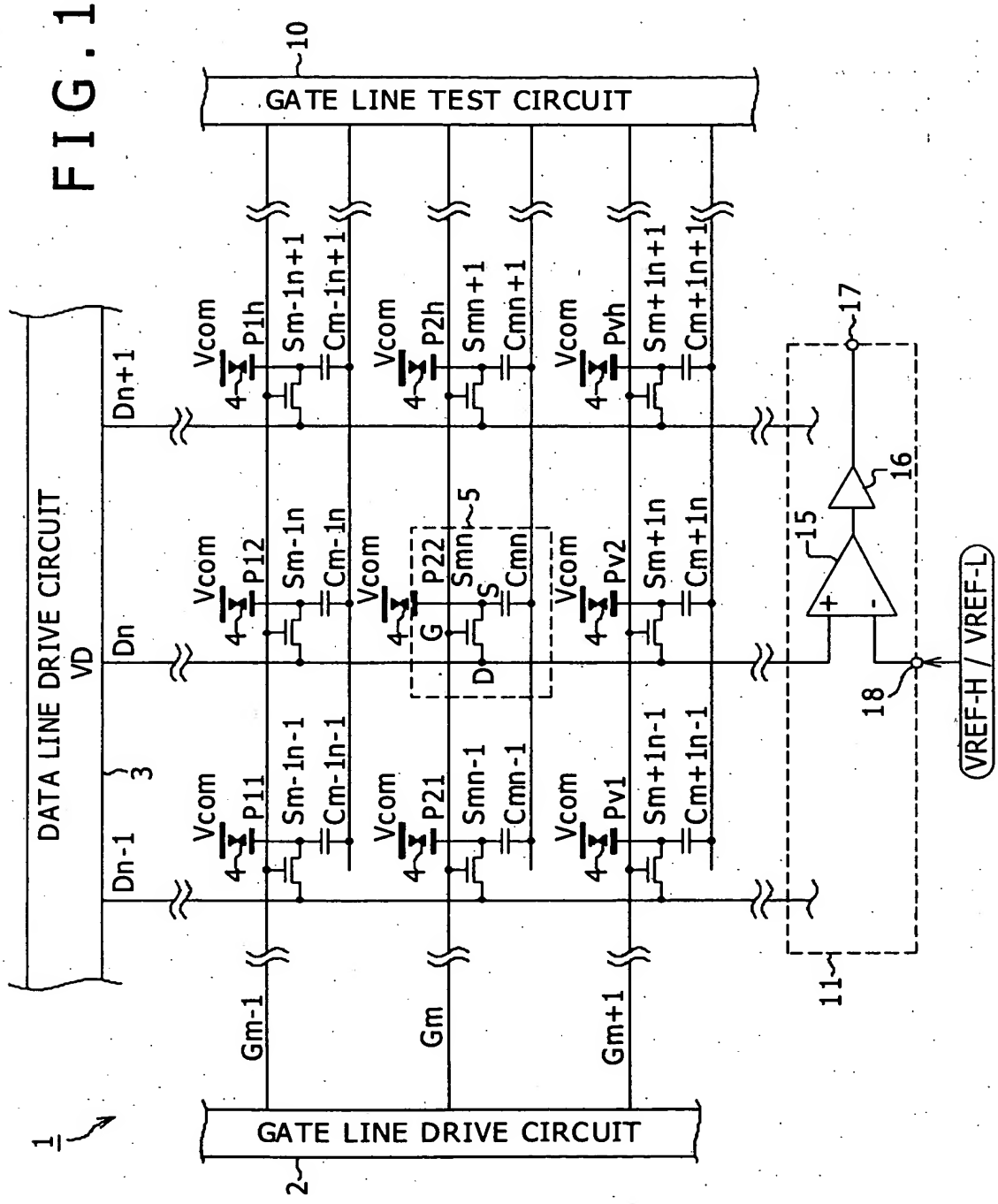

GATE LINE TEST CIRCUIT
10
DATA LINE DRIVE CIRCUIT
VH/VL
3
Dn+1
Dn
Dn-1
Vcom
P1h
P2h
Pvh
P12
P22
Pv2
P11
P21
Pv1
Sm-1n+1
Smn+1
Sm+1n+1
Sm-1n
Smn
Sm+1n
Sm-1n-1
Smn-1
Sm+1n-1
Cm-1n+1
Cmn+1
Cm+1n+1
Cm-1n
Cmn
Cm+1n
Cm-1n-1
Cmn-1
Cm+1n-1
G
S
D
5
4
17
16
15
VREF
11
Gm-1
Gm
Gm+1
GATE LINE DRIVE CIRCUIT
2
1

FIG. 12


GATE LINE TEST CIRCUIT
10
DATA LINE DRIVE CIRCUIT
VD
3
Dn+1
Dn
Dn-1
Vcom
P1h
P2h
Pvh
P12
P22
Pv2
P11
P21
Pv1
Sm-1n+1
Smn+1
Sm+1n+1
Cm-1n+1
Cmn+1
Cm+1n+1
Sm-1n
Smn
Sm+1n
Cm-1n
Cmn
Cm+1n
Sm-1n-1
Smn-1
Sm+1n-1
Cm-1n-1
Cmn-1
Cm+1n-1
4
5
G
S
D
Gm-1
Gm
Gm+1
GATE LINE DRIVE CIRCUIT
2
1
11
15
16
17
18
VREF-H / VREF-L